2017

FMC single chip adapter card

RD53A TESTING

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1. Introduction

The purpose of this document is to give a basic guideline for the use of the FMC card used for RD53A single chip testing. Schematics needed to understand this document, layout and Altium project with all the assembly details can be found in [RD53 twiki website].

This card is one of the PCBs needed for RD53A testing, being the interface between an FPGA board and the single chip card where the RD53A chip will be wire bonded. The main goal of this FMC adapter is to provide the interface needed to send commands from the FPGA to the single chip card and receive data from the chip. This is done via DisplayPort connectors. Also it provides JTAG connection with the SCC card for slow control of the chip and it includes LEMO connectors for receiving/transmitting trigger signals. Finally, it also has a multi-pin connector (QSH connector) making it capable of connecting with future daughter boards that would extend the capabilities of this board. Side A of the FMC card has the two display port connectors, JTAG connector and two LEMOs, while side be has the QSH connector and several jumpers for selecting options that will be explained in next sections (see Figures 2 and 3) All these features will be explained in the following sections.

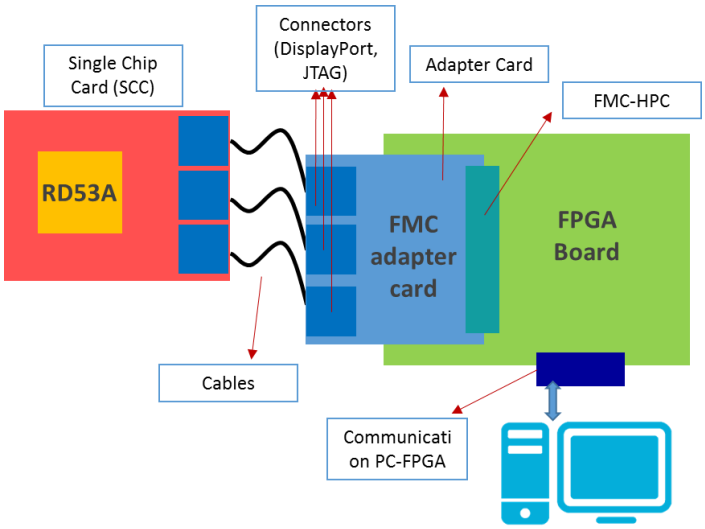

Figure 1: Test system general scheme.

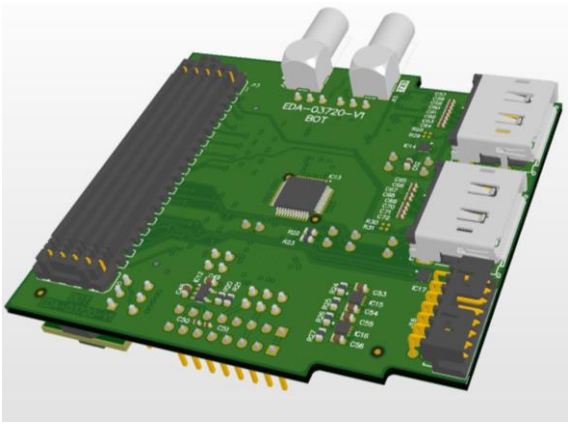

Figure 2: FMC adapter card picture, side A

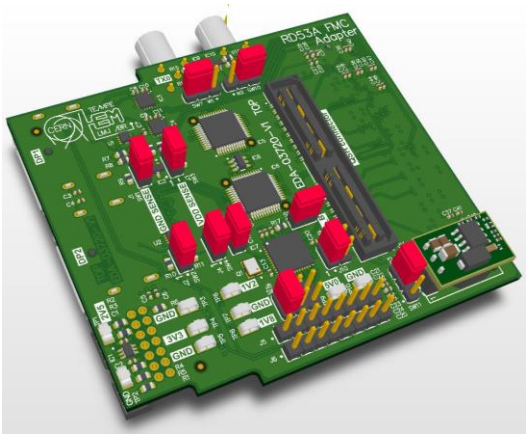

Figure 3: FMC adapter card picture, side B

2. FMC connector

The connection between FPGA card and FMC adapter is done via a high pin count FMC connector, that is divided in 10 columns (from A to K). All the signals received from the connectors are driven to the FPGA board via this connector. A brief explanation of the tags used for the signals connected to the FMC connector can be found in table 1. In the following sections these signals will be explained one by one.

Signal tag	Description
DP1	Signals coming from displayPort 1
DP2	Signals coming from displayPort 2
LEMO	Signals coming from LEMO connectors
TMS,TCK, TDO, TDI, TRST_B	Signals coming from JTAG connector
12V0	12.0V coming from FPGA board, pins C15 and 17.
3V3FPGA	3.3V coming from FPGA board, pins C39, D36, D38, D40
2V5	2.5V coming from FPGA board, pins E39, F40, G39, H40. It's also called VADJ or VFM in the FPGA board and it has to be selected with a jumper to this value. In XPressK7 FPGA board, this jumper is in the upper-right corner next to the battery. This jumper should only be moved when the board is switched off.
VREF	1.25V coming from FPGA. VREF=VFMC/2=VADJ/2=1.25V
SCL, SDA	Signals needed for I2C control
LOS_B, INTR_B, LOS_XAXB_B, LOL_B, CLKSYNC_CLKGEN, PLL_RST, GBTCLK_M2C, FPGA_CLK,	Signals related to the clock generation

Table 1: FMC connector nomenclature

3. DisplayPorts

DisplayPort connectors were chosen as the main connectors for sending commands from the FPGA and receiving data from the chip. Two displaPort connectors are used in this board. They are meant to be connected to displayPort connectors 1 and 2 in the SCC card (Single Chip Card). Section 3.1 explains the functionality of the displayPort connectors in SCC card, while section 3.2 explains the functionality of the displayPorts in FMC card.

3.1 DisplayPort connectors in SCC card:

Figures 4 and 5 shows the two displayPort connectors in the SCC card and the signals connected to them from the chip.

DisplayPort 1 in SCC card (DP1_SCC) drives the signals described in Table 2. If jumpers JP9 and JP11 in SCC are connected in the upper position, lines 1 to 12 in DP1_SCC drive the 4 differential data lanes from the chip to the FMC card. If jumper JP9 is connected in the down position, LANE2 in DP1_SCC is used to drive an external clock for the serializer in RD53A, coming from the FPGA board. If jumper JP11 is connected in the down position, LANE3 in DP1_SCC is used to drive an external clock for the CMD. Pins 13 and 14 are connected to an NTC resistor in order to measure the temperature of the

chip. Pins 16 and 17 are used for sending commands from the FPGA board, and pin 18 for sending the reset signal. Pins 19 and 20 are connected to VDDD and GND respectively in order to be able to measure these voltages levels. Notice that, for the differential signals, the polarity is inverted with respect the normal use of the displayPort connector. This was done in order to ease the routing of the signals in the PCB.

DisplayPort2 (DP2_SCC) in SCC card is used to drive signals described in table 3. Pins 1 to 12 are connected to the four differential signals called HITOR, and pin 15 and 17 are connected to auxiliary pins for probe card needs.

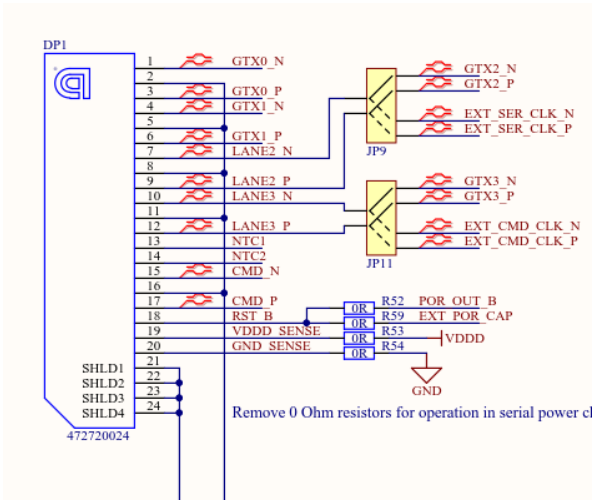

Figure 4: DisplayPort1 in SCC side

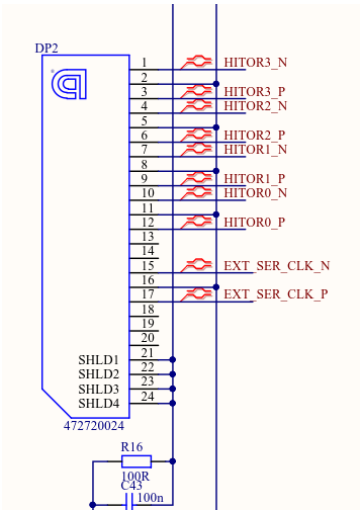

Figure 5: DisplayPort2 in SCC side

Pin	Original signals (names of the signals according to diplayPort standard)	SCC DP1, jumpers JP10 and JP11 in up position	Description	jumpers JP10 and JP11 in down position	Description
1	LANE0_P	GTX0_N	Data lane 0, negative polarity	GTX0_N	Data lane 0, negative polarity
2	GND	GND	Ground	GND	Ground
3	LANE0_N	GTX0_P	Data lane 0, positive polarity	GTX0_P	Data lane 0, positive polarity
4	LANE1_P	GTX1_N	Data lane 1 , negative polarity	GTX1_N	Data lane 1 , negative polarity
5	GND	GND	Ground	GND	Ground
6	LANE0_N	GTX1_P	Data lane 1, positive polarity	GTX1_P	Data lane 1, positive polarity
7	LANE2_P	GTX2_N	Data lane 2, negative polarity	EXT_SER_CLK_N	External clock for serializer, negative polarity
8	GND	GND	Ground	GND	Ground
9	LANE2_N	GTX2_P	Data lane 2, positive polarity	EXT_SER_CLK_P	External clock for serializer, positive polarity

10	LANE3_P	GTX3_N	Data lane 3, negative polarity	EXT_CMD_CLK_N	External clock for CMD, negative polarity
11	GND	GND	Ground	GND	Ground
12	LANE3_N	GTX3_P	Data lane 3, positive polarity	EXT_CMD_CLK_P	External clock for CMD, positive polarity
13	CONFIG1	NTC1	Connection with pin 1 of NTC resistor	NTC1	Connection with pin 1 of NTC resistor
14	CONFIG2	NTC2	Connection with pin 2 of NTC resistor	NTC2	Connection with pin 2 of NTC resistor
15	AUX_P	CMD_N	Command lane, negative polarity	CMD_N	Command lane, negative polarity
16	GND	GND	Ground	GND	Ground
17	AUX_N	CMD_P	Command lane, positive polarity	CMD_P	Command lane, positive polarity
18	Hot Plug Detect	RST_B	Reset line	RST_B	Reset line
19	DP_PWR_RETURN	VDDD_SENSE	Pin to measure VDD	VDDD_SENSE	Pin to measure VDD
20	DP_PWR	GND_SENSE	Pin to measure GND	GND_SENSE	Pin to measure GND

Table 2: DisplayPort1 signals in SCC

Pin	Original signals	SCC DP2	Description
1	LANE0_P	HITOR3_N	HITOR lane 3, negative polarity
2	GND	GND	Ground
3	LANE0_N	HITOR3 _P	HITOR lane 3, positive polarity
4	LANE1_P	HITOR2 _N	HITOR lane 2 , negative polarity
5	GND	GND	Ground
6	LANE0_N	HITOR2 _P	HITOR lane 2, positive polarity
7	LANE2_P	HITOR1 _N	HITOR lane 1, negative polarity
8	GND	GND	Ground
9	LANE2_N	HITOR1_P	HITOR lane 1, positive polarity
10	LANE3_P	HITOR0_N	HITOR lane 0, negative polarity
11	GND	GND	Ground
12	LANE3_N	HITOR0_P	HITOR lane 0, positive polarity
13	CONFIG1	N/C	Not connected
14	CONFIG2	N/C	Not connected
15	AUX_P	AUX_N	Auxiliary pin for wafer probing, negative polarity
16	GND	GND	Ground
17	AUX_N	AUX_P	Auxiliary pin for wafer probing, positive polarity
18	Hot Plug Detect	N/C	Not connected
19	DP_PWR_RETURN	N/C	Not connected
20	DP_PWR	N/C	Not connected

Table 3: DisplayPort2 signals in SCC

3.2 DisplayPort connectors in FMC card:

DisplayPort1 in FMC (DP1_FMC) can be connected to DP1_SCC, while DisplayPort2 in FMC card (DP2_FMC) can be used either to connect with DP1_SCC or DP2_SCC in SCC card, taking into account some changes in firmware. The main difference between receiving the data coming from DP1_SCC in DP1_FMC or DP2_FMC is the FPGA kind of receiver connected to the data lanes, either using the multi-gigabit transceivers of the Kintex 7 FPGA (called GTXs) or the general purpose receivers of the FPGA (called selectIOs).

3.2.0. DisplayPort cable

In order to understand the pinout assignment between SCC and FMC, one has to take into account that the pinout of sink side is reversed with respect the source side for the main data lanes. This is described in Figure 6. Also, as mentioned before, the polarity of signals in DP1_SCC and DP2_SCC is reversed respect the normal operation of displayPort (P->N and N->P) to ease the routing in SCC card.

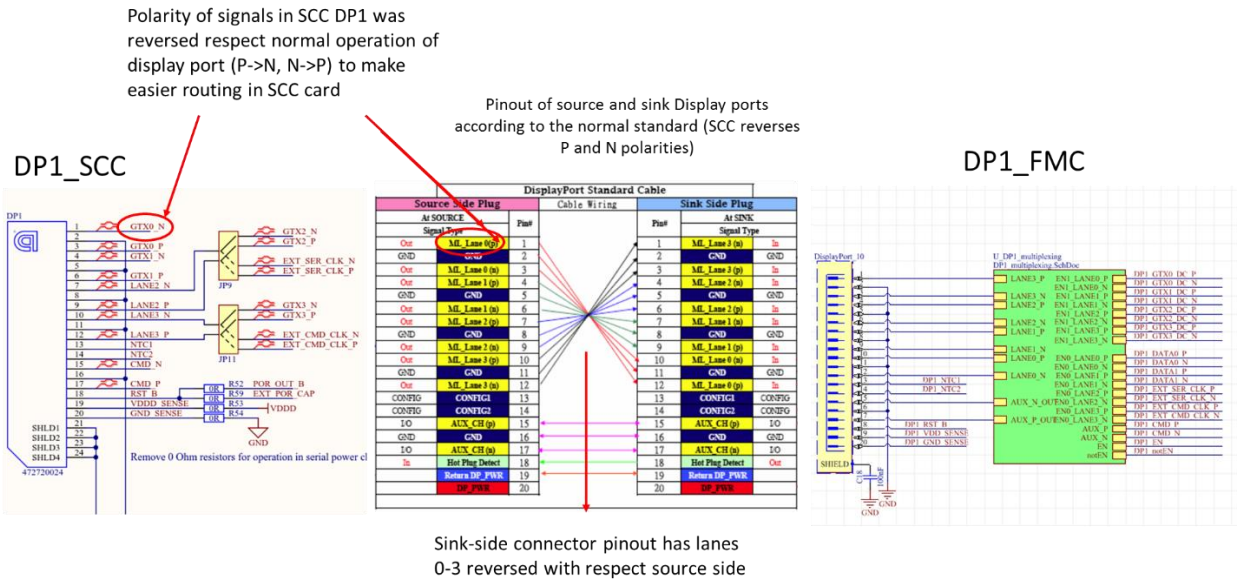

Figure 6: DisplayPort1 in SCC and FMC cards, connected by a DisplayPort cable, showing the reversion of the main lanes from source to sink side of the cable.

3.2.1.DisplayPort1 in FMC

Figure 7 shows a block diagram of the logic needed for the DP1_FMC and table 4 shows the names of the signals received in the DP1_FMC (taking into account the reversing scheme of the displayPort cable explained in section 3.2.0).

Pin	Original signals (names of the signals according to diplayPort standard)	DP1_FMC signals when JP10 and JP11 select data lanes	Description	DP1_FMC signals when JP10 and JP11 select external clocks	Description
1	LANE0_P	GTX0_N	Data lane 0, negative polarity	GTX0_N	Data lane 0, negative polarity
2	GND	GND	Ground	GND	Ground
3	LANE0_N	GTX0_P	Data lane 0, positive polarity	GTX0_P	Data lane 0, positive polarity
4	LANE1_P	GTX1_N	Data lane 1 , negative polarity	GTX1_N	Data lane 1 , negative polarity
5	GND	GND	Ground	GND	Ground
6	LANE0_N	GTX1_P	Data lane 1, positive polarity	GTX1_P	Data lane 1, positive polarity

7	LANE2_P	GTX2_N	Data lane 2, negative polarity	EXT_SER_CLK_N	External clock for serializer, negative polarity
8	GND	GND	Ground	GND	Ground
9	LANE2_N	GTX2_P	Data lane 2, positive polarity	EXT_SER_CLK_P	External clock for serializer, positive polarity
10	LANE3_P	GTX3_N	Data lane 3, negative polarity	EXT_CMD_CLK_N	External clock for CMD, negative polarity
11	GND	GND	Ground	GND	Ground
12	LANE3_N	GTX3_P	Data lane 3, positive polarity	EXT_CMD_CLK_P	External clock for CMD, positive polarity
13	CONFIG1	NTC1	Connection with pin 1 of NTC resistor	NTC1	Connection with pin 1 of NTC resistor
14	CONFIG2	NTC2	Connection with pin 2 of NTC resistor	NTC2	Connection with pin 2 of NTC resistor
15	AUX_P	CMD_N	Command lane, negative polarity	CMD_N	Command lane, negative polarity
16	GND	GND	Ground	GND	Ground
17	AUX_N	CMD_P	Command lane, positive polarity	CMD_P	Command lane, positive polarity
18	Hot Plug Detect	RST_B	Reset line	RST_B	Reset line
19	DP_PWR_RETURN	VDDD_SENSE	Pin to measure VDD	VDDD_SENSE	Pin to measure VDD
20	DP_PWR	GND_SENSE	Pin to measure GND	GND_SENSE	Pin to measure GND

Table 4: DisplayPort1 signals in FMC

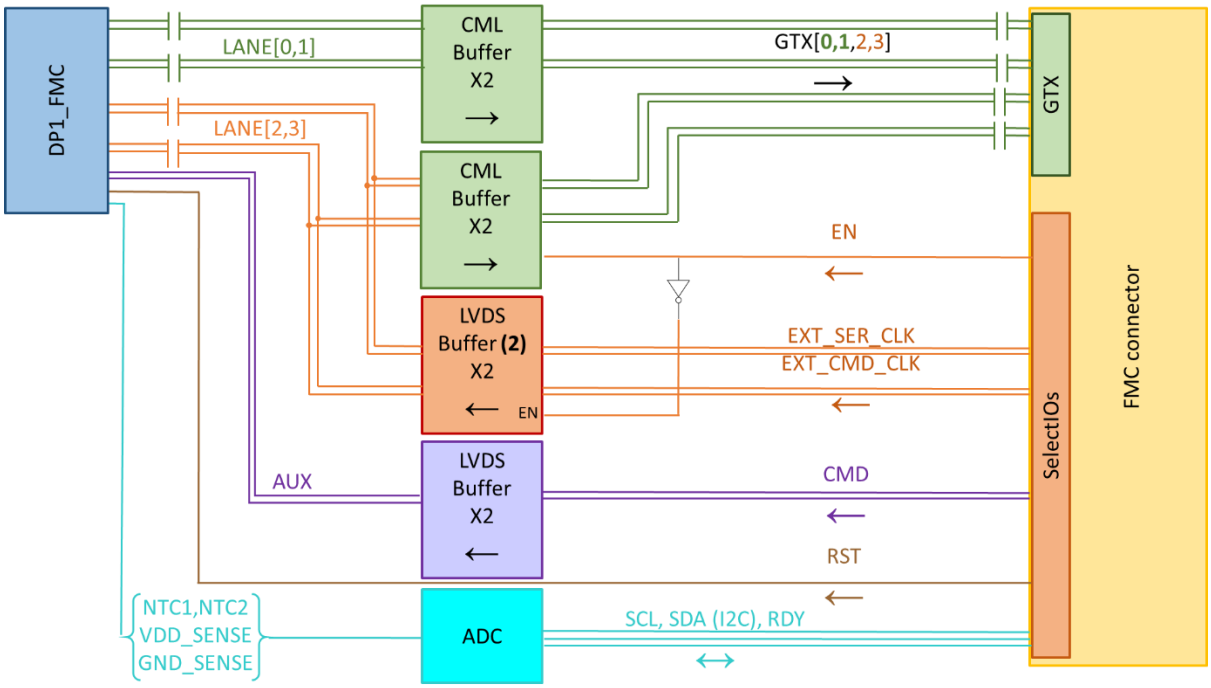

Figure 7: Block diagram of logic needed for DP1_FMC

If the jumpers JP10 and JP11 in SCC are selecting GTX2 and GTX3 signals (this will be called this DP1_OPERATION_MODE_1 in the rest of the document), all the data lines of DP1_FMC (GTX0 to GTX3) are connected to the multi gigabit transceivers of the FPGA, the GTXs. In between the DP1_FMC and the FMC connector, CML buffers are used (SY56216RMG), using AC coupling before and after the buffer (AC coupling before the buffer due to the serial powering scheme and after the buffer due to the requirements needed by the GTXs).

In case jumpers JP10 and JP11 in SCC are used to select EXT_SER_CLK or EXT_CMD_CLK, LANE2 and LANE3 in SCC side (corresponding to LANE0 and LANE3 in DP1_FMC due to the reversion in the order of the pins in the source of DP cable with respect the sink, see section 3.2.0) are used to send clocks from the FPGA to SCC. In order to do that, an LVDS buffer is used (DS90LV004TVS/NOPB, device IC5 in FMC schematics). This operation mode will be called DP1_OPERATION_MODE_2 in the rest of the document.

From firmware point of view, the selection of the operation mode is done via the enable signal DP1_EN connected to pin G22 in FMC connector. If DP1_EN is high, the LVDS buffer is powered off and DP1_OPERATION_MODE_1 is enabled. When DP1_EN is low, the LVDS buffer is powered on and the external clock signals EXT_SER_CLK and EXT_CMD_CLK can be sent to the chip (DP1_OPERATION_MODE_2).

The rest of the lanes in DP1_FMC are the same regardless of the operation mode. Pins 15 and 17 are used in order to send command from the FPGA to the SCC, using a LVDS buffer; pins 13 and 14 are connected to the NTC resistor pins in the SCC card, and are used to measure the temperature of the chip. They are connected to a voltage divider and then to an ADC that can be read out via I2C (ADC I2C address 1001000). Finally, pins 19 and 20 are connected to the ground and VDD in the SCC card, and are also connected to the ADC. They can be left floating by disconnecting jumpers J1 and J3 in FMC card for protecting the ADC in case of serial powering operation. More information of the NTC and ADC can be found in the appendix A.

3.2.2. DisplayPort2 in FMC

Figure 8 shows a block diagram for DP2_FMC and table 4 shows the pinout and description of each signal. DP2_FMC can be used to connect either to DP1_SCC or DP2_SCC. In this case the data lanes of the connector are connected to the general purpose transceivers of the FPGA (SelectIOs). LVDS drivers are used in between, and they can be enabled and disabled with DP2_EN signal. A similar scheme as the one used for the DP1_FMC is used here in order to be able to select the signals driven in main lanes 2 and 3 covering the different configurations set by jumpers JP10 and JP11 in SCC, either enabling the LVDS buffer 1 in Figure 8 for receiving the four data lanes, or enabling the buffer 2 and receiving two data lanes and sending external clocks (EXT_SER_CLK and EXT_CMD_CLK)

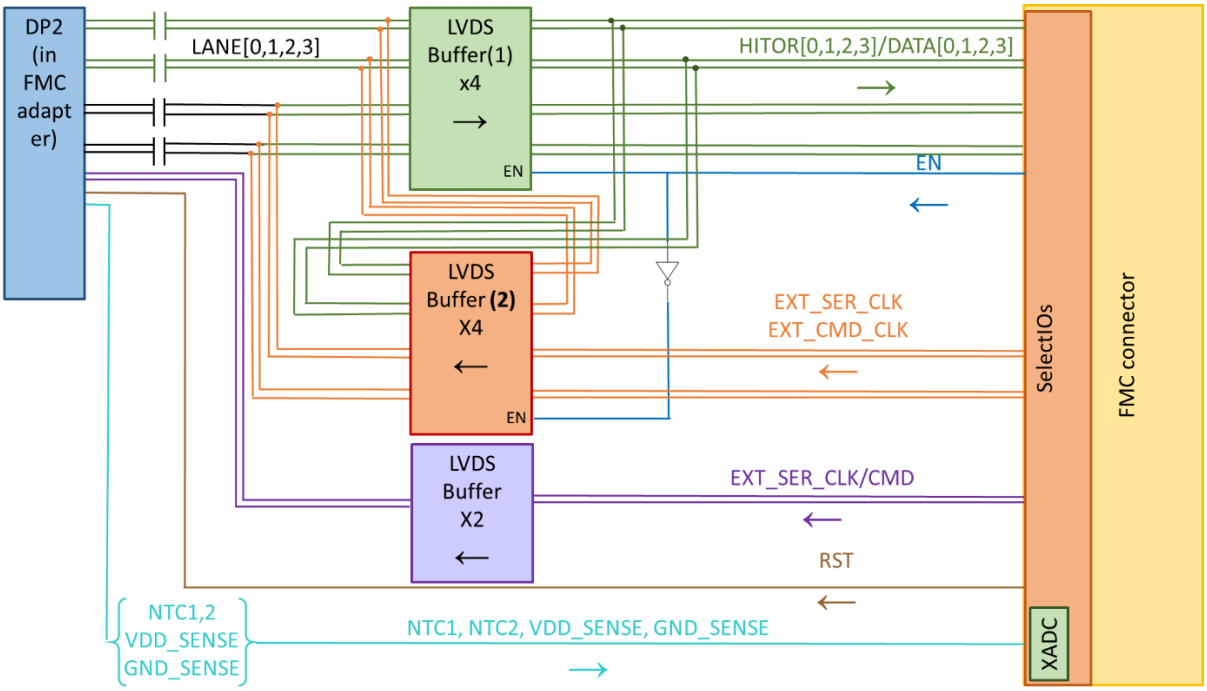

Figure 8: Block diagram of logic needed for DP2_FMC

		DP2_FMC signals when connected to DP1_SCC		DP2_FMC signals when connected to DP2_SCC
Pin	**Original signals (names of the signals according to diplayPort standard)**	**DP2_FMC signals when JP10 and JP11 select data lanes**	**DP2_FMC signals when JP10 and JP11 select external clocks**	**(No jumper selection in DP2_SCC)**
1	LANE0_P	GTX0_N	GTX0_N	HITOR3_N
2	GND	GND	GND	GND
3	LANE0_N	GTX0_P	GTX0_P	HITOR3 _P
4	LANE1_P	GTX1_N	GTX1_N	HITOR2 _N
5	GND	GND	GND	GND
6	LANE0_N	GTX1_P	GTX1_P	HITOR2 _P
7	LANE2_P	GTX2_N	EXT_SER_CLK_ N	HITOR1 _N
8	GND	GND	GND	GND

9	LANE2_N	GTX2_P	EXT_SER_CLK_P	HITOR1_P
10	LANE3_P	GTX3_N	EXT_CMD_CLK_N	HITOR0_N
11	GND	GND	GND	GND
12	LANE3_N	GTX3_P	EXT_CMD_CLK_P	HITOR0_P
13	CONFIG1	NTC1	NTC1	N/C
14	CONFIG2	NTC2	NTC2	N/C
15	AUX_P	CMD_N	CMD_N	AUX_N
16	GND	GND	GND	GND
17	AUX_N	CMD_P	CMD_P	AUX_P
18	Hot Plug Detect	RST_B	RST_B	N/C
19	DP_PWR_RETURN	VDDD_SENSE	VDDD_SENSE	N/C
20	DP_PWR	GND_SENSE	GND_SENSE	N/C

Table 5: DisplayPort2 signals in FMC

When DP2_FMC is connected to DP1_SCC, lanes 13, 14, 15, 17, 19 and 20 have the same functionality as when connecting DP1_FMC to DP1_SCC, but in this case the NTC pins, VDDD_SENSE and GND_SENSE are connected to the XADC drivers of the FPGA and not to an external ADC. Jumpers J4 and J2 in FMC can disconnect signals VDDD_SENSE and GND_SENSE in order to protect the FPGA from possible high voltage levels.

4. Clocking resources

The FMC card includes also a two output I2C programmable clock multiplier capable of generating two clock signals from 100Hz to 1028MHz (Si5342A-D-GM).

One of these clock outputs is used for the multi gigabit transceivers of the FPGA, as they need an external reference clock which frequency has to be adjusted according to the data rate of the input bit stream.

The second clock is connected to one of the MRCC receivers (Multi-Region Clock Capable receiver) of the FPGA for general purpose.

The clock multiplier has also 4 inputs that can be used to connect a crystal oscillator and use it as a clock reference for the multiplier. This is not mandatory, but reduces the jitter in the output clocks generated.

Finally, some control and signals are needed for different purposes, described in Table 6.

Signal	**Pin in clock multiplier**	**Pin in FMC connector**	**Description**
CLKSYNC_CLKGEN	43, 44	C18,C19	An external input clock can be used to synchronize its rising edge with the output clocks generated by the multiplier.
LOS_B	30	C10	Status bit monitoring input clock CLKSYNC_CLKGEN (Loss Of Signal)
LOL_B	27	C15	Loss Of Lock detection, asserted when the internal DSPLL has lost synchronization with the selected input clock.

LOS_XAXB_B	28	C14	Status bit monitoring the external crystal clock (Loss Of Signal)
INTR_B	33	C11	Interrupt pin, indicates a change in state of the status indicators (LOS, OOF, LOL, HOLD).
SDA, SCL	13,14	C30,C31	I2C signals for control of the device. I2C address 1101000
PLL_RST	17	C26	Active Low input that performs power-on reset of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up and can be left unconnected when not in use.

Table 6: Control signals for clock multiplier

Some jumpers are also used in order to select manually the voltage level of clocks and control signals, and also the input for synchronizing with an external clock. Table 7 summarizes the different options:

Jumpers	Name	Description
J8	**VDDO0,1** Output Clock Supply Voltage	Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTn outputs.
J10	**VDDS**, Status Output Voltage	The voltage on this pin determines VOL/VOH on the Si5342 LOL_A and LOL_B outputs. Connect to either 3.3 V or 1.8 V.
J7,J9	**IN_SEL0**, **IN_SEL1**, Manual input switching	Select one of the 4 CLKSYNC_CLKGEN possible inputs. In the first version of the board only IN_SEL0 is available (both jumpers disconnected)

Table 7: Jumpers needed for setting clock multiplier properties

5. LEMO connectors

Two LEMO connectors are included in the FMC card to be able to receive external triggers and send signals for handling communication with trigger control units. Both LEMOs are connected to single bit bus transceivers so both can either receive or send data. The input and output levels of the signal can be set with two different sets of jumpers to 1.8V, 2.5V, 3.3V or 5.0V, J5 for the input and J6 for the output.

6. JTAG

A JTAG connector is also included in the board in order to make the slow control of the RD53A by connecting it to the correspondent JTAG connector in the SCC card. Each line is connected to a bidirectional voltage level translator with automatic direction sensing, so the 2.5V signals coming from the FPGA can be translated to the 1.2V needed by the chip and vice versa.

7. QSH connector

A multi-pin connector is mounted in the side B of the FMC card in order to extend the input/output of the board with future daughter boards that can be plugged. The connector has two big metal plates, one of them is dedicated to ground and the other is connected to the 3.3V power line. All the pins in the connector can be used for general purpose with a daughter board except pins 1 and 3, that provide 1.25V from the FMC card, and pins 77 and 79 that provide 2.5V.

8. Power

As mentioned before, 12V, 3.3V, 2.5V and 1.25V power lines come from the FPGA card (see Table 1). However, more voltage values are needed for certain devices and applications. Three voltage regulators are used in the FMC board in order to obtain 1.2V, 1.8V and 5.0V.

These outputs can be adjusted with external resistors, so different values of these voltages can be obtained by changing these resistors (see equations in the schematics in order to do this, taking into account the limitations of the devices).

The 3.3V power line is used in most of the components of the FMC card. Depending on the board used and the power sources chosen in each FPGA board, this could lead to powering issues. In order to solve this, a DCDC converter (IC11, OKI-78SR-3.3/1.5-W36H-C) can be plugged to jumper J12, so the 3.3V powering all the board can be obtain either directly from the FPGA or with this DCDC converter. Jumper SW11 selects either of these options.

Appendix A: NTC thermistor

Properties of the NTC thermistor are explained in this section in order to make the voltage to temperature conversion from software. The ADC provides a difference of voltage between the terminals of the resistor, called V_{NTC}. R_1 is the resistor used in the voltage divider before the ADC, while the constant β and R_{25} are provided by the manufacturer. The temperature in the chip can be calculated with equation (1):

$$T = \frac{1}{\frac{1}{\beta} ln\left[\left(\frac{V_{NTC} \times R_1}{V - V_{NTC}}\right) / R_{T_2}\right] + \frac{1}{T_2}} \quad (1)$$

Where the value of the constants are:

β(K)	3435
R1 (kΩ)	39
V (V)	2.5
T2 (K)	298.15
RT2 (kΩ)	10
VNTC (V)	Measured by ADC

Table 8: constants for NTC thermistor

Table 9 shows a summary of values of the NTC thermistor for different temperatures:

T1(°C)	R_{NTC}(kΩ)
-20	77.5
-10	46.3
0	28.7
10	18.4

15	14.9
25	10.0
50	4.1
70	2.2
100	1.0

Table 9: resistance of NTC thermistor for different temperatures

Appendix B: summary of jumpers

Jumper ID	Description
J1	This jumper connects/disconnects the GND_SENSE pin from the DP1_SCC to the ADC in the FMC card.
J2	This jumper connects/disconnects the GND_SENSE pin from the DP2_SCC to the ADC in the FMC card.
J3	This jumper connects/disconnects the VDD_SENSE pin from the DP1_SCC to the ADC in the FMC card.
J4	This jumper connects/disconnects the VDD_SENSE pin from the DP2_SCC to the ADC in the FMC card.
J5	It sets the input/output voltage level for signals going from FPGA to transceivers IC9 and IC10.
J6	It sets the input/output voltage level for signals going from transceivers IC9 and IC10 to LEMOs J15 and J16.
J7	Selects one of the 4 CLKSYNC_CLKGEN possible inputs for the clock multiplier. In the first version of the board only IN_SEL0 is available (jumper disconnected)
J8	It selects the output voltage level (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTn, the clocks generated by the clock multiplier. Connect SW6 to pins 3 and 4 to have 2.5V output levels.
J9	Selects one of the 4 CLKSYNC_CLKGEN possible inputs for the clock multiplier. In the first version of the board only IN_SEL0 is available (jumper disconnected)
J10	The voltage on this pin determines VOL/VOH on the Si5342 LOL_A and LOL_B outputs. Connect to either 3.3 V or 1.8 V.
J12	Pins used to connect a DCDC converter to obtain the 3.3V source from the 12V FPGA power pins instead of using the 3.3V from the FPGA.
SW7	It sets the direction of signals going to transceiver IC9. Connect SW7 to VCCIO_A for signals going from FPGA to LEMO connector, or select SW7 to GND for signals coming from LEMO connector and going to FPGA.
SW10	It sets the direction of signals going to transceiver IC10. Connect SW10 to VCCIO_A for signals going from FPGA to LEMO connector, or select SW10 to GND for signals coming from LEMO connector and going to FPGA.
SW11	Selects whether the 3.3V are obtained from the FPGA or from the DCDC converter connected to pins J12.

Table 10: summary of jumpers in FMC card

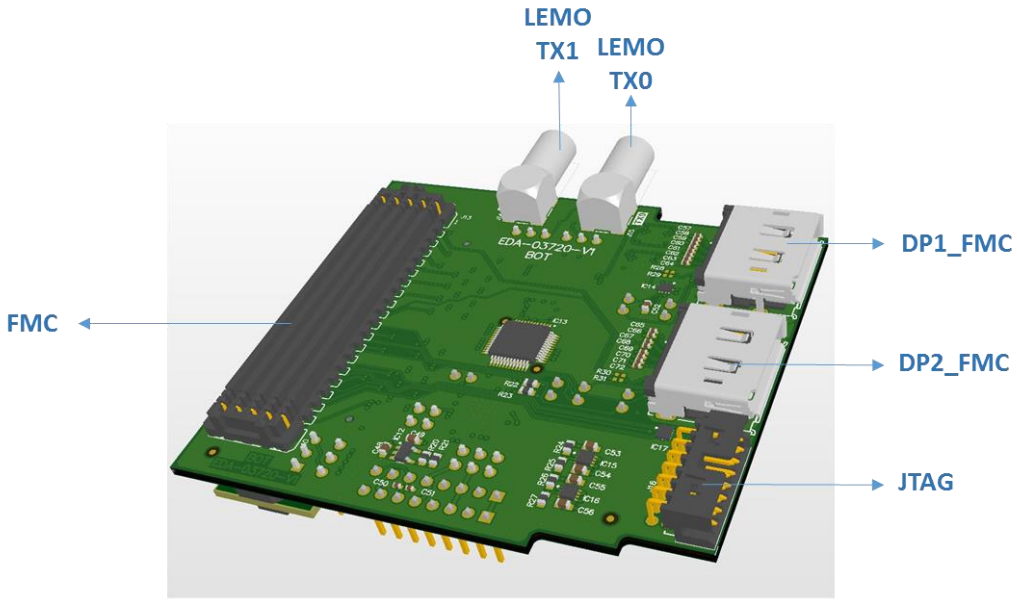

Figure 9: FMC card, connectors in side A

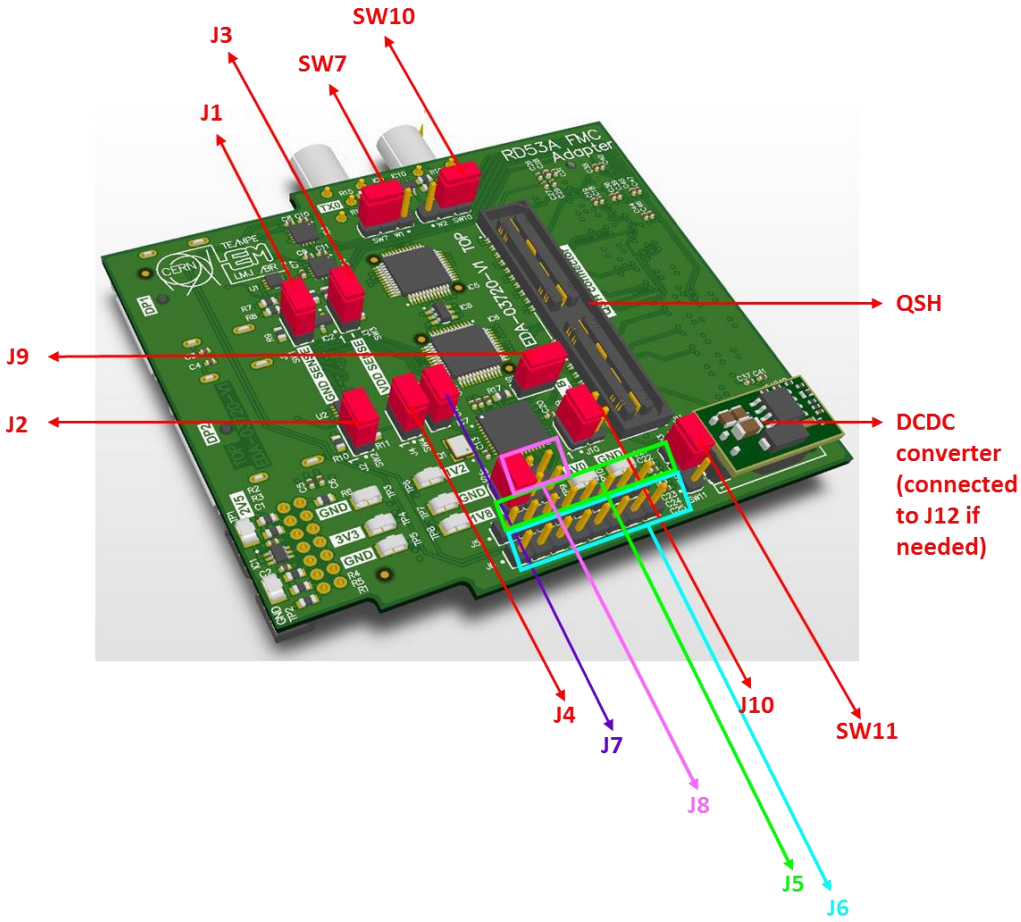

Figure 10: FMC card, jumpers and connectors in side B