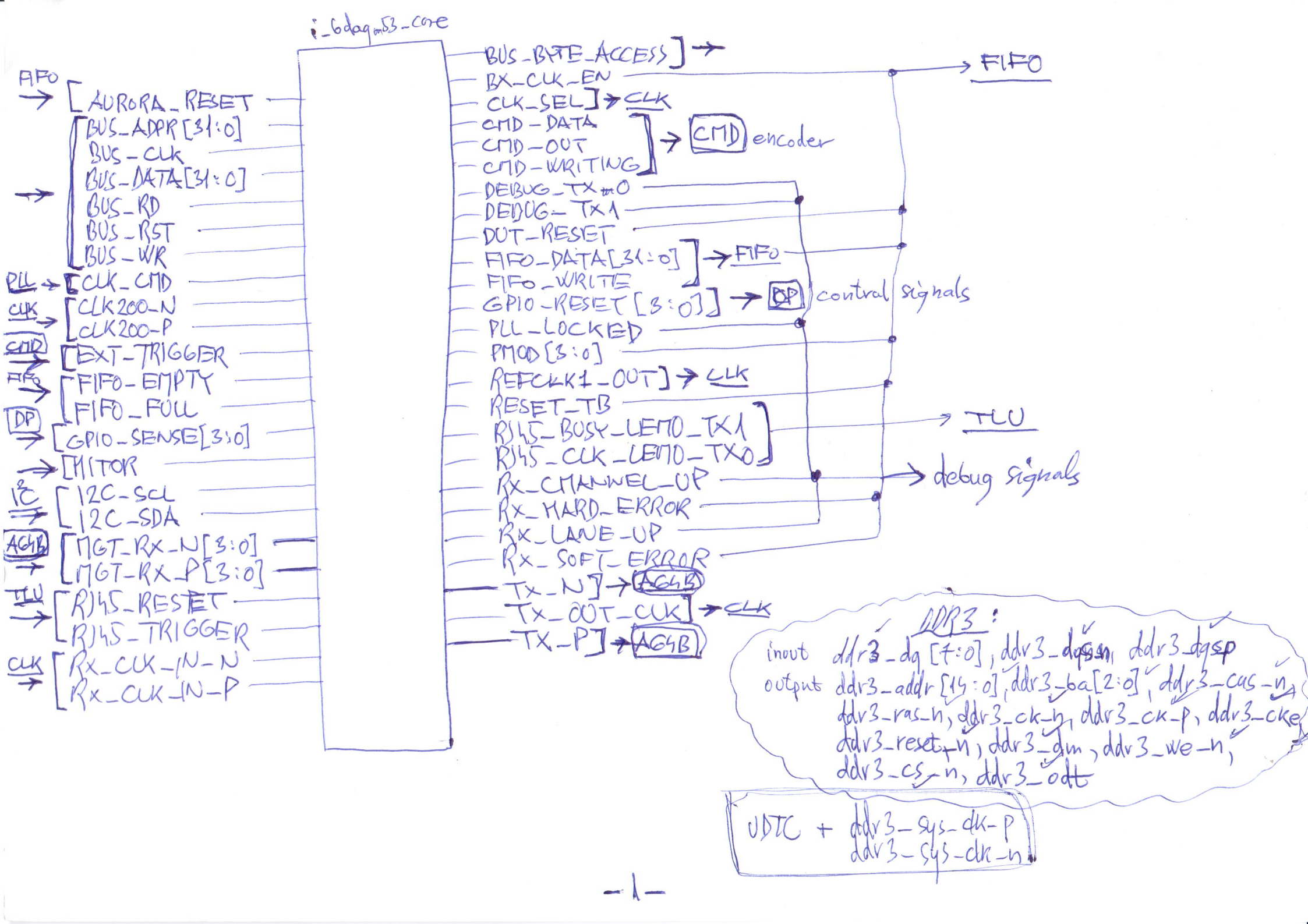
i_6dagm53_core
FIFO
AURORA_RESET
BUS_ADDR[31:0]
BUS_CLK
BUS_DATA[31:0]
BUS_RD
BUS_RST
BUS_WR
PLL
CLK_CMD
CLK
CLK200_N
CLK200_P
CMD
EXT_TRIGGER
FIFO
FIFO_EMPTY
FIFO_FULL
DP
GPIO_SENSE[3:0]
MITOR
I2C
I2C_SCL
I2C_SDA
AG4B
MGT_RX_N[3:0]
MGT_RX_P[3:0]
TLU
RJ45_RESET
RJ45_TRIGGER
CLK
RX_CLK_IN_N
RX_CLK_IN_P
BUS_BYTE_ACCESS
RX_CLK_EN
CLK_SEL
CLK
CMD_DATA
CMD_OUT
CMD_WRITING
CMD encoder
DEBUG_TX0
DEBUG_TX1
DUT_RESET
FIFO_DATA[31:0]
FIFO
FIFO_WRITE
GPIO_RESET[3:0]
DP
control signals
PLL_LOCKED
PMOD[3:0]
REFCLK1_OUT
CLK
RESET_TB
RJ45_BUSY_LEMO_TX1
RJ45_CLK_LEMO_TX0
TLU
RX_CHANNEL_UP
RX_HARD_ERROR
RX_LANE_UP
RX_SOFT_ERROR
debug signals
TX_N
AG4B
TX_OUT_CLK
CLK
TX_P
AG4B
DDR3 :
inout ddr3_dq[7:0], ddr3_dqsn, ddr3_dqsp
output ddr3_addr[14:0], ddr3_ba[2:0], ddr3_cas_n, ddr3_ras_n, ddr3_ck_n, ddr3_ck_p, ddr3_cke, ddr3_reset_n, ddr3_dm, ddr3_we_n, ddr3_cs_n, ddr3_odt
UDTC + ddr3_sys_clk_p, ddr3_sys_clk_n