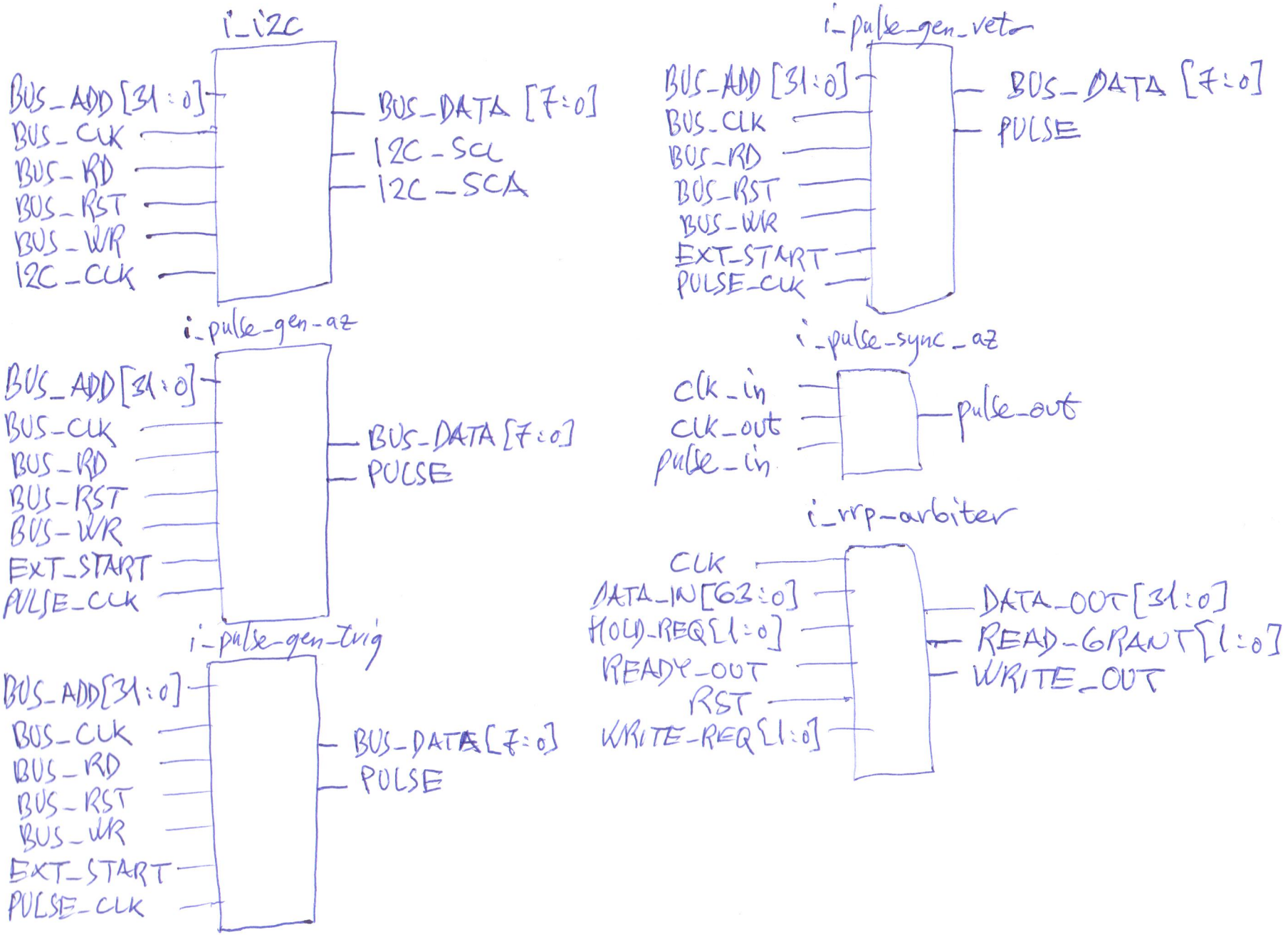
i_i2c
BUS_ADD [31:0]
BUS_CLK
BUS_RD
BUS_RST
BUS_WR
I2C_CLK
BUS_DATA [7:0]
I2C_SCL
I2C_SCA
i_pulse_gen_veto
BUS_ADD [31:0]
BUS_CLK
BUS_RD
BUS_RST
BUS_WR
EXT_START
PULSE_CLK
BUS_DATA [7:0]
PULSE
i_pulse_gen_az
BUS_ADD [31:0]
BUS_CLK
BUS_RD
BUS_RST
BUS_WR
EXT_START
PULSE_CLK
BUS_DATA [7:0]
PULSE
i_pulse_sync_az
clk_in
clk_out
pulse_in
pulse_out
i_pulse_gen_trig
BUS_ADD[31:0]
BUS_CLK
BUS_RD
BUS_RST
BUS_WR
EXT_START
PULSE_CLK
BUS_DATA[7:0]
PULSE
i_rrp_arbiter
CLK
DATA_IN[63:0]
HOLD_REQ[1:0]
READY_OUT
RST
WRITE_REQ[1:0]
DATA_OUT[31:0]
READ_GRANT[1:0]
WRITE_OUT